WHAT IS CLAIMED IS:

1. A high power MOSFET device; said device comprising a wafer of semiconductor material having a first surface and a parallel second surface; said first surface having a plurality of equally spaced symmetrically disposed polygonal source regions; a gate insulation layer on said first surface and disposed between said source regions; and a gate electrode on said gate insulation layer; a drain electrode on said second surface; and source electrode means connected to said polygonal source regions; a ring-shaped channel means of a first of the conductivity types disposed around the outer periphery of each of said polygonal source regions and beneath said gate insulation layer; one end of each of said channels being electrically connected to said source electrode means; the opposite end of each of said channels connected to respective regions which are centrally disposed beneath said gate insulation layer and which has the second of the conductivity types; a relatively high resistivity region of the second of the conductivity types underlying said common region and being continuous with said common region; said common region having a substantially higher conductivity than said underlying region; said common region and said underlying region being in series in the current path from said first and second source electrode means to said drain electrode.

2. The device of claim 1 wherein each of said source regions is hexagonal.

3. The device of claim 1 or 2 wherein each of said polygonal source regions has a relatively deep central region and a relatively shallow outer region; said relatively deep central region underlying said source electrode means.

4. A MOSFET device formed by D-MOS manufacturing techniques comprising, in combination:

a semiconductor chip;

a plurality of symmetrically disposed, polygonal source regions disposed on one surface of said chip and source electrode means connected to said source regions;

a gate electrode disposed between said spaced source regions and disposed on an insulation layer on top of said chip;

first and second channels disposed between the adjacent sides of each of said source regions and capable of being inverted by a gate bias; said first and second channels having spaced ends which extend into common respective semiconductor regions beneath said gate insulation layer; the opposite ends of said first and second channels connected to said source electrode means;

said first and second channels being of a first conductivity type and being capable of inversion to said second conductivity type; said common semiconductor region defining a current path across the thickness of said chip and having a high conductivity adjacent said surface of said chip and a low conductivity necessary for reverse voltage withstand ability at a depth greater than about one micron below said surface;

whereby said high conductivity region of said common region substantially decreases the on-resistance of said device.

5. The device of claim 4 wherein said chip has a bottom surface; said bottom surface having a drain electrode connected thereto.

6. The MOSFET of claim 5 wherein said first and second channels are the end regions of

respective relatively deep regions which extend away from one another and which have large outer radii of curvature.

7. The device of claim 4, 5 or 6 wherein said source regions are hexagonal.

8. The device of claim 1 or 4 wherein there are in excess of about 1,000 polygon source regions each having a width of about 1 mil.

9. The device of claim 8 wherein said source regions are hexagonal.

10. The device of claim 1 or 4 wherein each of said polygonal source regions has a width of about 1 mil.

11. The device of claim 8 wherein each of said polygon source regions has a width of about 1 mil.

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